ABSTRACT OF THE DISCLOSURE

A gate insulating layer, an amorphous silicon layer, a doped amorphous silicon layer and a Cr layer are sequentially deposited on a substrate on which a gate wire is formed. Next, the Cr layer is patterned to form a data line, a source electrode and a drain electrode. The doped amorphous silicon layer and the amorphous silicon layer are patterned at the same time, and the doped amorphous silicon layer is etched by using the data line, the source electrode and the drain electrode as etch stopper. Subsequently, a passivation layer is deposited and patterned to form a contact hole. An ITO layer is deposited and patterned to form a pixel electrode. According to the present invention, an oxide layer is prevented by performing a sequential deposition of the four layers in a vacuum state. As a result, the on current of the TFT is increased, and HF cleaning is not necessary because no oxide layer is formed. Therefore, the overall TFT manufacturing process is simplified.